What is claimed is:

1. A method to self update a firmware device, comprising:

receiving programming information from a communication interface; and

parsing the programming information into control commands and program data by a parser.

2. The method of claim 1 further comprising:

programming the firmware device based on the control commands by a control logic circuit; and

storing the program data to be written into the firmware device in a buffer.

3. The method of claim 2 further comprising:

providing the programming information to the parser by a source selector.

4. The method of claim 3 wherein providing the programming information comprises:

selecting one of the programming information from the communication interface and an input and output (I/O) channel data by a multiplexer; and

controlling a selection of the multiplexer by a multiplexer controller.

5. The method of claim 2 wherein programming the firmware device comprises:

erasing the firmware device by an erase control circuit; and

writing to the firmware device using the program data in the buffer by a write control circuit.

6. The method of claim 2 wherein the parsing comprises:

generating the control commands based on the parsed programming information by a state machine, the control commands including at least an erase command and a write command.

7. The method of claim 6 wherein the programming information includes at least a self-update identifier, program parameters, and the program data.

8. The method of claim 7 wherein generating the control commands comprises:

recognizing the self-update identifier;

reading the program parameters including at least erase and write addresses;

generating a buffer write command to write the program data into the buffer;

generating an erase command to the erase control circuit to a block in the firmware device at the erase address; and

generating a write command to the write control circuit to the program data in the buffer to the firmware device at the write address.

9. The method of claim 1 wherein receiving comprises:

converting serial data into the programming information by a serial to parallel converter.

10. The method of claim 5 wherein the I/O data channel is the low pin count (LPC) interface.

11. An apparatus to self update a firmware device, the apparatus comprising:

a communication interface to receive programming information; and

a parser coupled to the communication interface to parse the programming information into control commands and program data.

12. The apparatus of claim 11 further comprising:

a control logic circuit coupled to the parser to program the firmware device based on the control commands; and

a buffer coupled to the parser to store the program data to be written into the firmware device.

13. The apparatus of claim 12 further comprising:

a source selector coupled to the communication interface and the parser to provide the programming information to the parser.

14. The apparatus of claim 13 wherein the source selector comprises:

a multiplexer to select one of the programming information from the communication interface and an input and output (I/O) channel data; and

a multiplexer controller coupled to the multiplexer to control a selection of the multiplexer.

15. The apparatus of claim 12 wherein the control logic circuit comprises:

an erase control circuit to erase the firmware device; and

a write control circuit to write the firmware device using the program data in the buffer.

16. The apparatus of claim 12 wherein the parser comprises:

a state machine to generate the control commands based on the parsed programming information, the control commands including at least an erase command and a write command.

17. The apparatus of claim 16 wherein the programming information includes at least a self-update identifier, program parameters, and program data.

18. The apparatus of claim 17 wherein the state machine comprises:

a self-update identification state to recognize the self-update identifier;

a program parameters read state coupled to the self-update identification state to read the program parameters including at least erase and write addresses;

a program data buffer state to generate a buffer write command to write the program data into the buffer;

a block erasure state to generate the erase command, the erase command causing the erase control circuit to erase a block in the firmware device at the erase address; and

a block write state to generate the write command, the write command causing the write control circuit to write the program data in the buffer to the firmware device at the write address.

19. The apparatus of claim 15 wherein the communication interface includes a serial to parallel converter to convert serial data into the programming information.

20. The apparatus of claim 15 wherein the I/O data channel is the low pin count (LPC) interface.

21. A system comprising:

a host processor;

a firmware device; and

a self-update firmware controller coupled to the firmware device to self update the firmware device, the controller comprising:

a communication interface to receive programming information, and

a parser coupled to the communication interface to parse the programming information into control commands and program data.

22. The system of claim 21 wherein the controller further comprising:

a control logic circuit coupled to the parser to program the firmware device based on the control commands; and

a buffer coupled to the parser to store the program data to be written into the firmware device.

23. The system of claim 22 wherein the controller further comprising:

a source selector coupled to the communication interface and the parser to provide the programming information to the parser.

24. The system of claim 23 wherein the source selector comprises:

a multiplexer to select one of the programming information from the communication interface and an input and output (I/O) channel data; and

a multiplexer controller coupled to the multiplexer to control a selection of the multiplexer.

25. The system of claim 22 wherein the control logic circuit comprises:

an erase control circuit to erase the firmware device; and

a write control circuit to write the firmware device using the program data in the buffer.

26. The system of claim 22 wherein the parser comprises:

a state machine to generate the control commands based on the parsed programming information, the control commands including at least an erase command and a write command.

27. The system of claim 26 wherein the programming information includes at least a self-update identifier, program parameters, and program data.

28. The system of claim 27 wherein the state machine comprises:

a self-update identification state to recognize the self-update identifier;

a program parameters read state coupled to the self-update identification state to read the program parameters including at least erase and write addresses;

a program data buffer state to generate a buffer write command to write the program data into the buffer;

a block erasure state to generate the erase command, the erase command causing the erase control circuit to erase a block in the firmware device at the erase address; and

a block write state to generate the write command, the write command causing the write control circuit to write the program data in the buffer to the firmware device at the write address.

29. The system of claim 25 wherein the communication interface includes a serial to parallel converter to convert serial data into the programming information.

30. The system of claim 15 wherein the I/O data channel is the low pin count (LPC) interface.